Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A method for providing a synchronized clock signal having reduced jitter, the method comprising:

receiving a stable high frequency reference signal;

dividing said high frequency reference signal which allows a clock signal to have one of a plurality of clock phases;

receiving a pseudorandom number (PN) clock signal and providing PN phase adjustments of said received PN clock signal;

generating a tracking control signal in response to said PN phase adjustments for adjusting said clock phase to one of the plurality of available phases; and

adjusting said clock phase in accordance with the tracking control signal to provide said synchronized clock signal.

2. (Previously Presented) The method of claim 1, wherein said tracking control signal indicates the amount of the adjustment to make to said clock phase, wherein said adjustment can be in the positive or negative direction

3. (Previously Presented) The method of claim 1, wherein the tracking control signal indicates the number of adjustments to make to said clock phase, wherein said adjustment can be in the positive or negative direction.

4. (Previously Presented) The method of claim 1 further comprising:

multiplying said high frequency reference signal prior to dividing said high frequency reference signal.

5. (Previously Presented) The method of claim 1 wherein said high frequency signal is provided using a temperature compensated crystal oscillator.

6. (Previously Presented) A base station (BS), the BS comprising:

circuitry configured to receive a stable high frequency reference signal;

a divider to divide said high frequency reference signal which allows a clock signal to have one of a plurality of clock phases;

circuitry configured to receive a pseudorandom number (PN) clock signal and to provide PN phase adjustments of said received PN clock signal;

circuitry configured to generate a phase adjustment signal to adjust clock phase to one of the plurality of available phases; and

circuitry configured to adjust said clock phase in accordance with the phase adjustment signal to provide said synchronized clock signal.

7. (Previously Presented) The BS of claim 1 wherein said tracking control signal indicates the amount of the adjustment to make to said clock phase, wherein said adjustment can be in the positive or negative direction

8. (Previously Presented) The BS of claim 1, wherein the tracking control signal indicates the number of adjustments to make to said clock phase, wherein said adjustment can be in the positive or negative direction.

9. (Currently Amended) A remote network <u>terminal</u> ~~terminals~~ (RNT), the RNT comprising:

circuitry configured to receive a stable high frequency reference signal;

a divider to divide said high frequency reference signal which allows a clock signal to have one of a plurality of clock phases;

circuitry configured to receive a pseudorandom number (PN) clock signal and to provide PN phase adjustments of said received PN clock signal;

circuitry configured to generate a phase adjustment signal to adjust a clock phase to one of the plurality of available phases; and

circuitry configured to adjust said clock phase in accordance with the phase adjustment signal to provide said synchronized clock signal.

10. (Previously Presented) The RNT of claim 1 wherein said tracking control signal indicates the amount of the adjustment to make to said clock phase, wherein said adjustment can be in the positive or negative direction

11. (Previously Presented) The RNT of claim 1, wherein the tracking control signal indicates the number of adjustments to make to said clock phase, wherein said adjustment can be in the positive or negative direction.